



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/518,286

07/05/2005

Paul R. Routley

30740/285906

6677

4743

7590

11/13/2008

MARSHALL, GERSTEIN & BORUN LLP
233 S. WACKER DRIVE, SUITE 6300
SEARS TOWER
CHICAGO, IL 60606

EXAMINER

HO, BAO QUAN T

ART UNIT

PAPER NUMBER

2629

MAIL DATE

DELIVERY MODE

11/13/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/518,286

Applicant(s)

ROUTLEY ET AL.

Examiner

BAO-QUAN T. HO

Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 August 2008.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 4-13 and 15-29 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1, 4-13 and 15-29 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 16 December 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB08)
Paper No(s)/Mail Date 04/04/2008
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1, 4-5, 10-11, 13, 15-16, 19-20, 22, and 26-27** are rejected under 35 U.S.C. 102(b) as being anticipated by Sakamoto, US Patent 5,594,463.

Regarding claim 1, Sakamoto discloses in Fig. 6 a display driver control circuitry for controlling a display driver for an electroluminescent display (30), the display comprising at least one electroluminescent display element (52), the driver including at least one substantially constant current generator (constant current source 88, col. 6 lines 56-59) for driving the display element, the control circuitry comprising:

a drive voltage sensor (terminal A, col. 7 lines 7-14) for sensing a voltage on a first line (A0) in which the current is regulated by said constant current generator; and

a voltage controller (CPU 54, col. 7 lines 14-20) coupled to said drive voltage sensor for controlling the voltage of a supply (Vd) for said constant current generator in response to said sensed voltage, and configured to control said supply voltage to increase the efficiency of said display driver,

wherein said voltage controller (54) is configured to reduce said supply voltage (driving voltage Vd reduced by the estimated voltage drop Vf of the EL element, col. 7 lines 40-46) when this will not substantially reduce said regulated current and/or said

display brightness (the driving current value is set S102, which is the brightness, while the voltage drop is to be detected S110 by setting the drive current fixed to estimate the voltage drop across the anode and cathode of the EL element to configure the driving voltage Vd, col. 7 lines 18-61), and

said voltage controller (54) is configured to control said supply voltage (Vd) such that said constant current generator (88) operates in the vicinity of its compliance limit (driving current value is set S102, col. 7 lines 24-25).

Regarding claim 4, Sakamoto discloses further in Fig. 11 comprising means to determine a compliance limit for use by said voltage controller (CPU 54 outputs current command for the constant current source 88 to be controlled at an appropriate value, col. 9 lines 54-63).

Regarding claim 5, Sakamoto discloses further in Fig. 6 and 7 comprising a supply voltage sensor (Terminal B, S108 and S110, col. 7 lines 47-50) for sensing said supply voltage (Vd), and means to determine a difference between said supply voltage (voltage Vd at the electric source) and said first line voltage (the voltage Vx that is increased in the highest degree), and wherein said voltage controller is configured to control said supply voltage responsive to said difference (step S114, col. 7 lines 51-61).

Regarding claim 10, Sakamoto discloses wherein said display has at least one control line (lines coming from PWM 48-0, 48-1, etc..., col. 6 lines 56-67 to col. 7 lines 1-6) for controlling the illumination of said at least one electroluminescent display element (52), wherein said drive voltage sensor is configured to sense the voltage on said display control line (terminal A), and wherein said voltage controller (82) has an

output for controlling an adjustable power supply configured for providing said supply voltage.

Regarding claim 11, Sakamoto discloses in Fig. 2 and 6 a display driver (X driver 32, col. 5 lines 15-19) including the display driver control circuitry of claim 1.

Regarding claim 13, Sakamoto discloses in Fig. 6 and 7 a method of reducing the power consumption of a display driver driving an electroluminescent display (30), the display comprising at least one electroluminescent display element (52), the driver (X driver 32) including at least one substantially constant current generator (constant current source 88, col. 6 lines 56-59) for driving the display element and having a power supply for supplying power at a supply voltage for said current generator, the method comprising:

sensing (terminal A, col. 7 lines 7-14) a voltage on a first line coupled to the current generator, the current in which first line is regulated by the current generator; and

controlling (CPU 54) said supply voltage responsive to said sensed voltage (V_x) to reduce said supply voltage (driving voltage V_d reduced by the estimated voltage drop V_f of the EL element, col. 7 lines 40-46) when a reduction may be made without substantially altering said regulated current brightness (the driving current value is set S102, which is the brightness, while the voltage drop is to be detected S110 by setting the drive current fixed to estimate the voltage drop across the anode and cathode of the EL element to configure the driving voltage V_d , col. 7 lines 18-61) and

such that said supply voltage (Vd) such that said current generator operates at or near its compliance limit (driving current value is set S102, col. 7 lines 24-25).

Regarding claim 15, Sakamoto discloses in Fig. 11 determining said current generator compliance limit for use in said controlling (CPU 54 outputs current command for the constant current source 88 to be controlled at an appropriate value, col. 9 lines 54-63).

Regarding claim 16, Sakamoto further discloses a method comprising:

sensing (Terminal B, S108 and S110, col. 7 lines 47-50) a voltage on a second line (K0), the voltage on said second line being dependent upon said power supply voltage (Terminal B is used to measure the voltage drop across the EL element depending on the supply voltage on line A0); and

determining (S108 and S110, col. 7 lines 47-50) a voltage difference between the voltage sensed on said first (voltage Vx is increased to the highest degree) and second (voltage Vd at the electric source) lines;

wherein said controlling is responsive to said voltage difference (step S114, col. 7 lines 51-61).

Regarding claim 19, Sakamoto discloses a method wherein said display has at least one control line (lines coming from PWM 48-0, 48-1, etc..., col. 6 lines 56-67 to col. 7 lines 1-6) for controlling the illumination of said at least one electroluminescent display element, wherein said driver (X driver 32, Fig. 6) drives said control line, and wherein said sensing (detection Terminal A) comprises sensing a voltage on said control line.

Regarding claim 20, Sakamoto discloses a method wherein a said substantially constant current generator comprises a current source (constant current source 88).

Regarding claim 22, Sakamoto discloses in Fig. 2 and 6 a method wherein said display comprises a passive matrix display having a plurality of electroluminescent display elements (52) and a plurality of row electrodes (K0, K1, etc...) and a plurality of column electrodes (K0, K1, etc...) for addressing said display elements, and wherein said driver (X driver 32) is coupled to at least one of said plurality of row electrodes (K0, K1, etc...) and said plurality of said column electrodes (A0, A1, etc...) for driving said display.

Regarding claim 26, Sakamoto discloses a carrier carrying processor control code (ROM 58 connected to CPU 54, Fig. 5) to implement the method of claim 13.

Regarding claim 27, Sakamoto discloses a Display driver circuitry (X driver 32, col. 5 lines 15-19) configured to implement the method of claim 13

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. **Claims 6-7, 12, 17-18, 25, and 28-29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Everitt, US Pub. 2002/0167471.

Regarding claim 6, Sakamoto discloses in Fig. 6 wherein said display has a plurality of electroluminescent display elements (52), and wherein said display driver has a plurality of substantially constant current generators (88) for simultaneously driving said plurality of display elements, each said constant current generator being configured for regulating the current on an associated display drive line (A0, A1, etc...), and wherein said voltage controller (82) configured to control said supply voltage (Vd) responsive to the sensed voltage (Vx) on a said drive line having a maximum voltage of said drive line sensed voltages (step S108 in Fig. 7, col. 7 lines 47-50).

Sakamoto does not specially teach the display driver control circuitry further comprising a drive voltage sensor for sensing the voltage on each said display drive line.

However, Everitt teaches in Fig. 4 and 7 a display driver control circuitry further comprising a drive voltage sensor for sensing the voltage on each said display drive line (Voltage drivers 304 connected to each column and also a calibration circuit 338 , Page 3 in Paragraph [0034], to measure the voltages from each column, Page 5 in Paragraph [0055]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have used a calibration circuit for measuring voltage for each of the driving line as taught by Everitt in place of the drive voltage sensor of Sakamoto for the purpose of power reduction for the display (Page 5 in Paragraph [0064]).

Regarding claim 7, Sakamoto discloses further in Fig. 7 comprising a supply voltage sensor (Terminal B, S108 and S110, col. 7 lines 47-50) for sensing said supply voltage (V_d), and means to determine a difference between said supply voltage (voltage V_d at the electric source) and said maximum voltage (the voltage V_x that is increased in the highest degree), and wherein said voltage controller is configured to control said supply voltage responsive to said difference (step S114, col. 7 lines 51-61).

Regarding claim 12 and 25, Everitt discloses wherein said electroluminescent display element comprises an organic light emitting diode (Page 1 in Paragraph [0004]).

Regarding claim 17, Sakamoto disclose the method as claimed in claim 13, Sakamoto also discloses wherein said display comprises a plurality of simultaneously driveable electroluminescent display elements (52) each being driven by a said substantially constant current generator (88), each said substantially constant current generator having an associated drive line the current in which is regulated by the current generator(A0, A1, etc...), the method further comprising:

As taught by Everitt, sensing the voltage on each said associated drive line (Everitt discloses in Fig. 4 and 7 a plurality of voltage drivers 304 with a calibration circuit 338, Page 3 in Paragraph [0034], to sense the voltage on each drive line, Page 5 in Paragraph [0055]. The motivation to combine as mentioned above in claim 6, thus combining Sakamoto with Everitt would meet this limitation); and

Sakamoto further discloses controlling (CPU 54) said supply voltage responsive to said sensed voltage (V_x) to reduce said supply voltage (driving voltage V_d reduced by the estimated voltage drop V_f of the EL element, col. 7 lines 40-46) when a reduction

may be made without substantially altering the regulated current (the driving current value is set S102, which is the brightness, while the voltage drop is to be detected S110 by setting the drive current fixed to estimate the voltage drop across the anode and cathode of the EL element to configure the driving voltage V_d , col. 7 lines 18-61) in a said associated drive line having a maximum sensed voltage (V_x is to be detected to the highest degree in step S108, col. 7 lines 47-50).

Regarding claim 18, Sakamoto further discloses a method comprising:

sensing (Terminal B, S108 and S110, col. 7 lines 47-50) a voltage on a further line (K0), the voltage on said further line being dependent upon said power supply voltage (Terminal B is used to measure the voltage drop across the EL element depending on the supply voltage on line A0); and

determining (S108 and S110, col. 7 lines 47-50) a voltage difference between the voltage sensed on said further line (voltage V_d at the electric source) and said maximum sensed voltage (voltage V_x is increased to the highest degree); and

wherein said controlling is responsive to said voltage difference (step S114, col. 7 lines 51-61).

Regarding claim 28, Sakamoto further discloses a maximum voltage detect module to detect said maximum voltage of said drive line sense voltages (S/H circuit 74 receives the signal from the sensing terminals, FIG. 5 and Col. 6 lines 16-21).

Regarding claim 29, Sakamoto discloses where said maximum voltage detect module comprises a peak detect circuit to detect a peak said sensed voltage on a said drive line, and wherein said peak detect circuit is coupled to a sample/hold circuit (S/H

circuit 74 is used to detect the voltage on the drive line, although Sakamoto does not mentioning the S/H circuit 74 having a peak detect circuit, however it is commonly known for a sample and hold circuit to use a capacitor, a peak detect circuit, to sample an analog data at any desire period of time with the use of a switch that alternates to connect and disclose the analog data from the capacitor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to recognize a S/H circuit 74 taught by Sakamoto would have a peak detect circuit for the purpose of data tracking).

5. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Everitt as applied to claim 6 above, and further in view of Koyama, US Patent 6,730,966.

Regarding claim 8, Sakamoto in view of Everitt discloses a display driver control circuitry according to claim 6, Sakamoto also discloses in Fig. 6 wherein said display comprises a passive matrix display, but Sakamoto in view of Everitt does not specifically discloses wherein said voltage controller is configured to control said supply voltage on a frame-by-frame basis.

However, Koyama teaches wherein a voltage controller is configured to control said supply voltage on a frame-by-frame basis. (Koyama discloses in Fig. 5 in col. 11 lines 24-27, a controller 112 is set to turn on the EL driver voltage during each subframe).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have used the controller to turn on the EL driver voltage during each subframe as taught by Koyama to be applied to the controller of Sakamoto for the purpose of preventing a decrease in the number of gradations (col. 5 lines 25-33).

6. **Claim 24** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Koyama.

Regarding claim 24, Sakamoto discloses the method according to claim 22. Furthermore, Claim 24 will be rejected on the same basis in view of Koyama as applied with the motivation is stated above in claim 8. Thus, the combination of Sakamoto with Koyama meets the method of sensing and controlling on a frame-by-frame basis.

7. **Claim 9** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Everitt as applied to claim 6 above, and further in view of Young et al. (hereafter referenced as Young), US Patent 5,075,596).

Regarding claim 9, Sakamoto in view of Everitt discloses a display driver control circuitry according to claim 6, Sakamoto also discloses in Fig. 6 wherein said display comprises a passive matrix display having a plurality of rows of display elements, but

Sakamoto in view of Everitt does not specifically disclose wherein said voltage controller is configured to control said supply voltage on a row-by-row basis.

However, Young teaches wherein a voltage controller is configured to control said supply voltage on a row-by-row basis. (Young discloses in col. 3 lines 41-45 an adjustment to the effective pixel voltage of an electroluminescent display on a row by row basis)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have modified the controller to be configured to control said supply voltage on a row-by-row basis as taught by Young to be applied to the controller of Sakamoto for the purpose of increasing the contrast ratio of gray shades which improves the video quality of electroluminescent displays (col. 3 lines 45-51).

8. **Claim 23** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Young.

Regarding claim 23, Sakamoto discloses the method according to claim 22. Furthermore, Claim 23 will be rejected on the same basis in view of Young as applied as applied with the motivation is stated above in claim 9. Thus, the combination of Sakamoto with Young meets the method of sensing and controlling on a row-by-row basis.

9. **Claim 21** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Rutherford, US Patent 6,861,810.

Regarding claim 21, Sakamoto discloses the method according to claim 13, but does not specifically teaches wherein a said substantially constant current generator comprises a current sink.

However, Rutherford teaches in Fig. 4 a substantially constant current generator comprises a current sink (col. 4 lines 37-39).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have used a current sink as taught by Rutherford rather than the current source of Sakamoto for the purpose of driving the electroluminescent depending on the way the diodes are arranged in the display structure (col. 4 lines 37-39).

Response to Arguments

10. Applicant's arguments filed 08/01/2008 have been fully considered but they are not persuasive.

On the last page in the second paragraph, applicant argues "the word 'compliance' does not appear anywhere in the description or claims of Sakamoto" and in the amended claim 1, "which recites 'a voltage controller... configured to control said constant current generator operates in the vicinity of its compliance limit' is neither disclosed nor suggested by Sakamoto", and similar to amended claim 13. Examiner disagrees, Sakamoto discloses the voltage controller is used to control the constant current generator in compliance limit (CPU 54 controls the constant current source 88 in

a compliance limit, current command, to work in normal operations, Col. 4 lines 64-65 and Col. 6 lines 48-55).

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BAO-QUAN T. HO whose telephone number is (571)270-3264. The examiner can normally be reached on M-F, 8:30 am to 5:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh D. Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BTH

/Chanh Nguyen/
Supervisory Patent Examiner, Art
Unit 2629